

**REMARKS**

Applicant respectfully requests reconsideration of the subject application as amended. In response to the office action mailed 12/22/04, Applicant is submitting this amendment with the filing of an RCE. Claims 26 and 27 are currently pending.

In the latest office action, the Examiner continues to reject claims 20-23 and 25 under 35 U.S.C. §102(b) and claim 24 under 35 U.S.C. §103(a), citing Bechade (US Patent 5,789,966) for all of the rejections.

Applicant submits that the new claims recite language that clearly distinguish over Bechade in that the claimed embodiments of the invention recite a multiplexer circuit that does not employ a buffer between the between the first node and the first input terminal of the NAND gate, as well as between the second node and the second input terminal of the NAND gate. The direct coupling language is now recited clearly to claim that this feature reduces time delay for an eight bit width input to the multiplexer.

Bechade discloses a distributed (in spatial separation) multiplexer in which buffered inverters 24 are used to optimize performance of the multiplexer of Figure 1 (Bechade at col. 4, lines 16-23). The inverters are used to buffer the output of the multiplexer to restore fast signal transition time (col. 4, lines 1-14). The claimed embodiments of the invention utilize direct coupling at the output (without an output buffer/inverter) to reduce gate delay. A buffer (inverter) is not employed, since the multiplexer need not necessarily be a distributed multiplexer (as in Bechade). Accordingly, Applicant submits that this feature is now clearly recited in new claims 26 and 27.

Accordingly, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §102(b) and 35 U.S.C. §103(a) rejections and allow claims 26 and 27.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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